A 0.7V Time-based Inductor for Fully Integrated Low Bandwidth Filter Applications

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***Abstract*—A time-based gyrator is presented to implement active inductors in an area efficient manner. Using a ring oscillator to integrate the input voltage and a switched transconductor to inject current into the input node, the proposed gyrator achieves inductive input impedance without using either large resistors or capacitors. Realizing the gyrator in this manner makes it amenable for technology scaling. Fabricated in 65 nm CMOS process, the inductor operates from a 0.7 V supply voltage and consumes 528 μW. Measurement results show inductance values in the range of 150 μH to 1.5 mH can be achieved.**

***Index Terms*–active inductor, gyrator, VCO, time-domain signal processing, ring oscillator**

I. Introduction

Technology scaling over the past several decades has helped to greatly reduce active device dimensions. However, scaling has not necessarily resulted in similar scaling of passive circuit elements such as the resistor, capacitor, and the inductor, which typically occupy a significant fraction of total chip area [1]. While resistors and capacitors may have enjoyed some scaling benefits, density of inductors has by and large remained the same and as a result they continue to take up large fractions of die area. In view of this, the focus of this paper is to explore active inductor topologies that facilitate realization of very large inductances without using either large resistors or capacitors. Specifically, we focus on low-Q inductor applications such as filtering as opposed to power conversion applications that require very high Q inductors.

Active inductor can be implemented using a gyrator [2], as depicted in Fig. 1(a). It consists of an integrator formed by $\mathrm{G_{MF}}$-C that acts on the input voltage, $\mathrm{V_{in}}$, and a transconductor $\mathrm{G_{MB}}$, that converts the integrator output voltage to current, $\mathrm{I_{in}}$. The impedance presented by this circuit is inductive as illustrated by the below equation:

$$\mathrm{Z_G} = \frac{\mathrm{V_{IN}}}{\mathrm{I_{IN}}} = \frac{\mathrm{sC}}{\mathrm{G_{MF}G_{MB}}} \longrightarrow \widehat{\mathrm{L}} = \frac{\mathrm{C}}{\mathrm{G_{MF}G_{MB}}} \qquad (1)$$

Ideally, this technique can be used to implement a wide range of inductance values with significantly less area compared to a passive inductor. However, in practice, implementing large inductance poses many design challenges. First, very large capacitor or a very small transconductance is needed to increase inductance. Because minimum transconductance is limited by the smallest bias current that can be generated reliably, inductors used in very low bandwidth applications such as EEG, EMG, or EKG signal acquisition systems [3], [4] would require large capacitors and would end up occupying significant area.

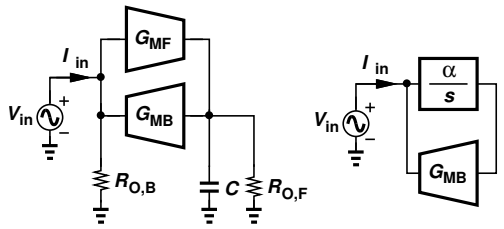

Fig. 1. (a) Classical gyrator based *active inductor* and (b) block-level implementation of the *active inductor*.

Second, finite output impedance $\mathrm{R_{O,F}}$, of the transconductor makes the integrator lossy and the integrator behaves as an amplifier for frequencies below $1/\mathrm{R_{O,F}C}$ [5]. Increasing $\mathrm{R_{O,F}}$ in scaled processes is difficult. Third, linearity of transconductors is severely compromised under low supply voltage, which limits useful linear range of the inductor. It is important to note that despite the appearance of a loop, it suffers from concerns such as saturation of the integrator.

In view of these challenges, we seek to explore alternate implementations of the gyrator. We propose to replace $\mathrm{G_M}$-C integrator in a classical gyrator with a time-based integrator that is immune to many of the aforementioned design challenges. Using a voltage-controlled ring oscillator (VCO) as the integrator allows to achieve infinite DC gain (lossless integration) and take full benefit of technology scaling [6].

II. Proposed Inductor

A simplified block diagram of the proposed time-based inductor is shown in Fig. 2. It is composed of two multi-phase voltage controlled oscillators ($\mathrm{VCO_{IN}}$, $\mathrm{VCO_{REF}}$), a bank of phase detectors and switched transconductors. Because input control voltage of the VCO changes its frequency, VCO acts as an ideal voltage to phase integrator [7]. Denoting voltage-to-frequency gain of the VCO by $\mathrm{K_{VCO}}$, integrator transfer function, $\mathrm{H_{VCO}(s)}$, equals:

$$\mathrm{H(s)} = \frac{\Phi_{\mathrm{VCO}}(\mathrm{s})}{\mathrm{V_{IN}(s)}} = \frac{\mathrm{K_{VCO}}}{\mathrm{s}} \qquad (2)$$

Therefore, a VCO can be used in the feed-forward path (see Fig. 2) in place of the $\mathrm{G_M}$-C integrator to implement a gyrator.

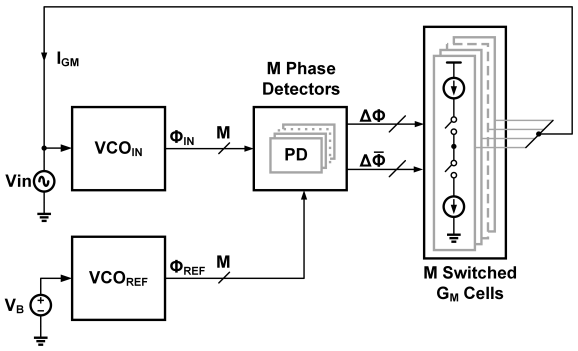

Fig. 2. Block diagram of the proposed active inductor.

To this end, $\mathrm{VCO_{IN}}$ output phase is converted to a pulse-width modulated signal by a phase detector (PD) by comparing $\mathrm{VCO_{IN}}$ phase with that of $\mathrm{VCO_{REF}}$. Assuming free-running frequencies of both the VCOs are equal, pulse width of the PD output is proportional to the phase of $\mathrm{VCO_{IN}}$ and can be represented as:

$$\mathrm{V_{PWM}} = \int \mathrm{V_{IN}}(\tau)\mathrm{d}\tau = \frac{\mathrm{V_{IN}K_{VCO}K_{PD}}}{\mathrm{s}} \tag{3}$$

A switched transconductor converts 2-level PD output into current which is then injected into the input node, to make the input impedance inductive as expressed by the the below equations:

$$\mathrm{I_{G_M}} = \frac{\mathrm{V_{in}K_{VCO}K_{PD}G_M}}{\mathrm{s}} \tag{4}$$

$$\frac{\mathrm{V_{in}}}{\mathrm{I_{G_M}}} = \mathrm{sL} \longrightarrow \mathrm{L} = \frac{1}{\mathrm{K_{VCO}K_{PD}G_M}} \tag{5}$$

Plotting Eq. 5 as shown in Fig. 3, reveals the possibility of realizing large inductors without either using large capacitors or very small transconductors. While driving the transconductor with a 2-level PD output makes them inherently linear, it also introduces undesirable spurious tones in the vicinity of multiples of $\mathrm{F_{VCO}}$ [8]. We seek to suppress these tones by a using a multi-phase ring oscillator. By taking M phases out of $\mathrm{VCO_{REF}}$ and $\mathrm{VCO_{IN}}$, we generate an M level $\mathrm{V_{PWM}}$ signal, which results in pushing the spurious tones to $\mathrm{M \cdot F_{VCO,IN}}$ [7], where they can be easily filtered. M-level $\mathrm{V_{PWM}}$ signal is generated by comparing M phases of $\mathrm{VCO_{IN}}$ with corresponding M phases of $\mathrm{VCO_{REF}}$ using M phase detectors. The M PWM signals are fed to M switched transconductors whose outputs are shorted to perform the desired current summation.

The proposed time-based gyrator suffers from a lower bound on $\mathrm{F_{IN}}$. To elucidate this, consider the case when a sinusoidal signal with an amplitude of $\mathrm{V_{IN}}$ and frequency $\mathrm{F_{IN}}$ is applied at the input. The resulting amplitude of the induced phase swing equals:

$$\Delta\Phi_{\mathrm{IN}} = \frac{\mathrm{V_{IN}K_{VCO}}}{\mathrm{F_{IN}}} \leq 2\pi \tag{6}$$

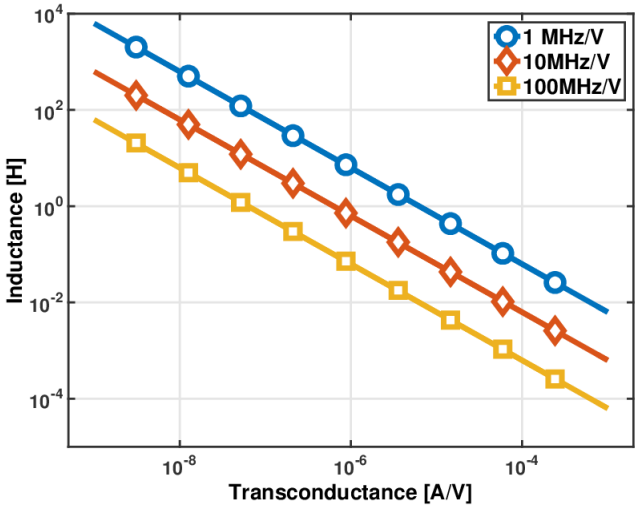

Fig. 3. Transconductance range compared to maximum inductance for various $\mathrm{K_{VCO}}$ values.

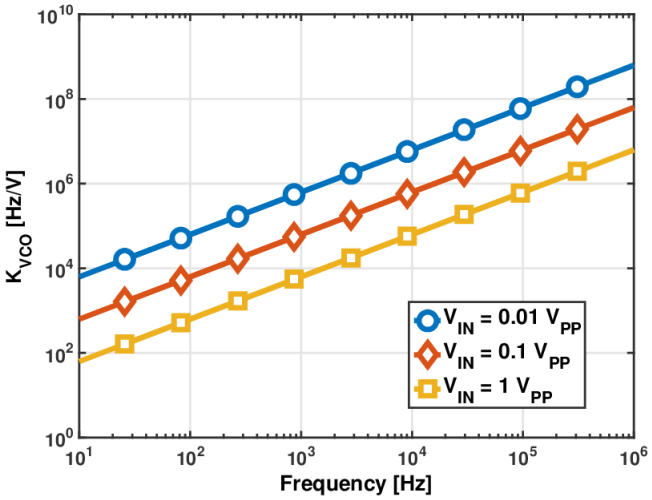

Fig. 4. Required $\mathrm{K_{VCO}}$ values for minimum input frequencies across various input swings to ensure distortion free performance.

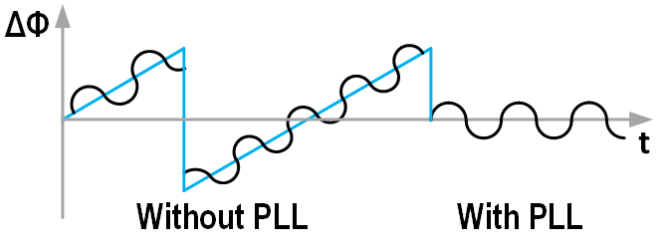

Fig. 5. Phase detector output waveforms, showing the effect of phase detector saturation.

$\Delta\Phi_{\mathrm{IN}}$ must be smaller than the PD input range, which is 2π in our implementation. Exceeding this range will saturate the PD and the gyrator loses its inductive behavior. This relationship is shown in Fig. 4 for various input amplitude

and frequencies.

We have thus far assumed free running frequencies of $\mathrm{VCO_{IN}}$ and $\mathrm{VCO_{REF}}$ to be equal. However, in practice, it is difficult to guarantee this in the presence of mismatches. Any offset between $\mathrm{F_{REF}}$ and $\mathrm{F_{IN}}$ will cause the phase to accumulate indefinitely, eventually saturating the phase detector (see Fig. 5). To mitigate this, we propose to frequency lock the two oscillators using a a low bandwidth phase-locked loop (PLL).

PLL can also be used to alleviate the PD saturation issue described above by setting the PLL bandwidth slightly larger than the minimum encountered $\mathrm{F_{IN}}$ in a given application. When $\mathrm{F_{IN}}$ is within the PLL bandwidth, $\mathrm{VCO_{IN}}$ ceases to behave like an integrator resulting in $\mathrm{I_{in}}$ being proportional to $\mathrm{V_{in}}$ (ref. Fig. 1(b)). Thus, for signals with frequencies within the PLL bandwidth the proposed topology behaves like a resistor. However, when $\mathrm{F_{IN}}$ falls outside the PLL's bandwidth, $\mathrm{VCO_{IN}}$ starts to behave as an integrator up until $\approx \mathrm{F_{VCO}}/10$ and the proposed topology behaves like a lossless inductor.

III. Building Blocks

A. VCO and phase detector

The VCO is implemented using a 11-stage ring oscillator. Single-ended delay stages are used to minimize area and power. The number of stages are decided based on the requirement to push the PWM tones to at least a decade higher, which requires a minimum of 10 equally spaced phases. Since a single-ended VCO requires odd number of stages, 11 delay cells are used. Each of the delay stages are implemented as a cascade of 3 inverters and an AC-coupled buffer is used to increase the swing to full-scale before driving the PD.

Each VCO is tuned through two digitally-controllable current sources. One source sets the DC bias current to adjust the center frequency of the oscillator, while the other source is controlled by $\mathrm{V_{IN}}$. Both inputs are tunable by setting a digital word that controls the number of active fingers for each current source. Both the center frequency and $\mathrm{K_{VCO}}$ are tunable by over an order of magnitude. The same VCO is used for both the input and reference oscillators. The reference oscillator uses a control voltage generated by the PLL instead of $\mathrm{V_{IN}}$.

Outputs of $\mathrm{VCO_{IN}}$ and $\mathrm{VCO_{REF}}$ are fed to two-state PDs implemented using two cross-coupled D flip-flops and an XOR-gate as shown in Fig. 6(a). The PD output, $\mathrm{V_{PWM}}$, is proportional to the phase-error, $\Delta\Phi = \Phi_{\mathrm{IN}} - \Phi_{\mathrm{REF}}$ and periodic with period 2π as shown in Fig. 6(b), resulting in a PD gain of $\mathrm{K_{PD}} = 0.7/2\pi$ V/rad.

B. Switched-$\mathrm{G_M}$ Cell

Fig. 7 shows the schematic of the switched $\mathrm{G_M}$ cell. It consists of two 4-bit digitally programmable current sources $\mathrm{I_1}$ and $\mathrm{I_2}$, current-steering switches $\mathrm{M_1}$ to M_4, and cascode current-mirrors $\mathrm{M_5}$ to $\mathrm{M_8}$. The current-steering switches are controlled by the PWM signal $\mathrm{V_{PWM}}$ and $\overline{\mathrm{V_{PWM}}}$. Current-steering is preferred over on-off current sources (ref. Fig. 2) to minimize the current glitch at the output. The strength of the $\mathrm{G_M}$ cell is not only tunable by a 4-bit digital word but also by changing the bias voltage controlling $\mathrm{I_1}$ and $\mathrm{I_2}$. The devices are sized for a peak current of approximately 50 μA per cell. All $\mathrm{G_M}$ cells have their outputs tied together to form a current summer.

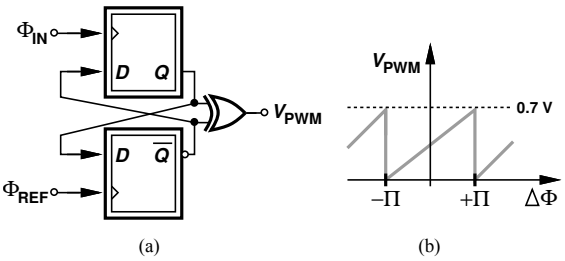

Fig. 6. Two-state phase detector (a) schematic and (b) transfer characteristic.

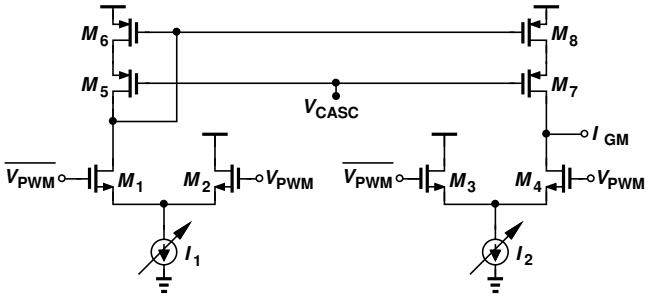

Fig. 7. Switched $\mathrm{G_M}$ cell schematic.

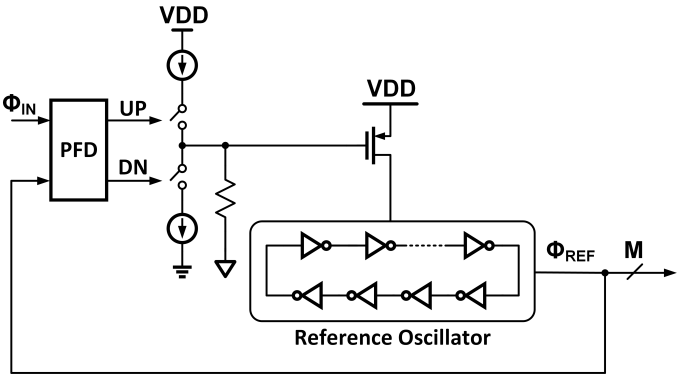

Fig. 8. Schematic of Type-I PLL used to provide bias voltage for reference oscillator.

C. Low bandwidth PLL

Fig. 8 shows the type-I PLL used in the proposed architecture to overcome the phase wrapping problem described in Section II. We use a NAND-based phase-frequency detector (PFD) to measure phase error. The corresponding UP and DN signals drive a charge-pump, which is implemented using the same switched $\mathrm{G_M}$ cell described in Section III-B. The resistor has an externally applied common mode voltage, which combined with the charge-pump current, generates the control voltage driving the PMOS of $\mathrm{VCO_{REF}}$. This sets the frequency of the reference oscillator equal to the common mode input oscillator frequency.

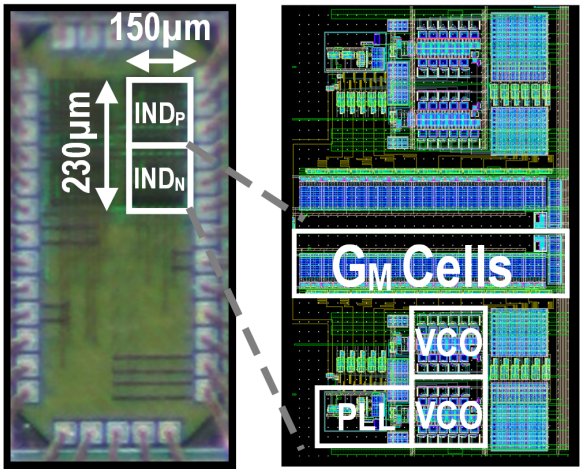

Fig. 9. Die photo.

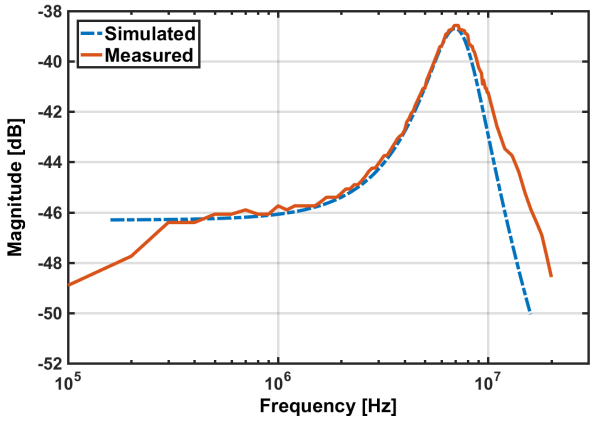

Fig. 10. Measurement and simulated magnitude response of a passive RLC filter using the proposed inductor of 480 μH.

We deliberately use a type-I PLL whose bandwidth is set to the lowest frequency that the inductor can maintain saturation-free performance. This allows the inductor to "degrade gracefully", as the impedance goes from inductive to resistive as the frequency lowers. We also do not want true phase tracking, as that would prevent any integration from the input to output of the forward path, as the input and reference phases would be locked. While use of a type-II PLL would allow us to have lower bandwidth with the same loop gain, it would come at the cost of large area. We note that if multiple inductors were required on the same chip, for example in applications that use filter banks, only a single PLL is required.

IV. Measurement Results

The time-based active inductor is implemented in 65 nm CMOS technology and occupies an active area of 0.017 mm^2. A die micrograph is shown in Fig. 9. The power consumption at a center frequency of 180 MHz is 528 μW under no load condition, of which the time-domain circuitry (two VCOs and PLL) consume 514 μW. The digital control circuits consume 4 μW, and the G_M cell bias circuits consume 10 μW of power.

Inductor's performance is measured by putting it in a passive RLC filter. Demonstrated here is an inductance of 480 μH with an operating frequency of 180 MHz. Operating at this frequency range, the inductor performs as expected for an input frequency range of 500 kHz to 20 MHz. The input voltage swing seen by the inductor is 70 mV_{pp}. A simulated transfer function is compared with the measured results in Fig. 10. Measurement results show inductance values in the range of 150 μH to 1.5 mH can be achieved.

V. Conclusion

A time-based gyrator is presented to implement active inductors in an area efficient manner. Using a ring oscillator to integrate the input voltage and a switched transconductor to inject current into the input node, the proposed gyrator achieves inductive input impedance without using either large resistors or capacitors. Realizing the gyrator in this manner makes it amenable for technology scaling. Fabricated in 65 nm CMOS process, the inductor operates from a 0.7 V supply voltage and consumes 528 μW. Measurement results show inductance values in the range of 150 μH to 1.5 mH can be achieved. We note that our implementation realizes only a one-port (grounded) inductor, and realizing a true two-port floating inductor is the future scope of our work.

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